A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO

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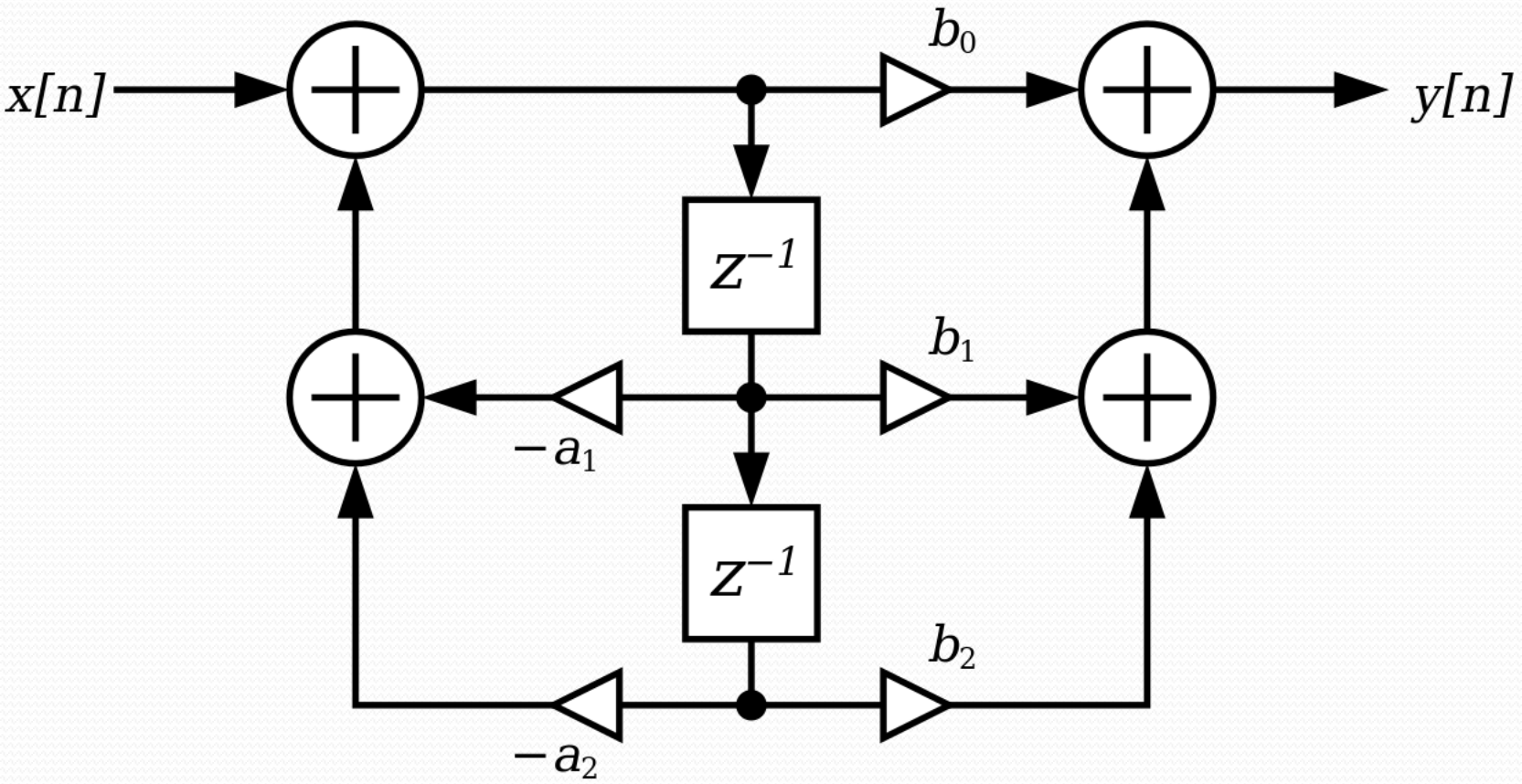
Abstract

- Nowadays, many applications require simultaneous computation of multiple independent fast Fourier transform (FFT) operations with their outputs in natural order.
- Therefore, this brief presents a novel pipelined FFT processor for the FFT computation of two independent data streams.
- The proposed architecture is based on the multipath delay commutator FFT architecture.
- It has an *N*/2-point decimation in time FFT and an *N*/2-point decimation in frequency FFT to process the odd and even samples of two data streams separately.
- The main feature of the architecture is that the bit reversal operation is performed by the architecture itself, so the outputs are generated in normal order without any dedicated bit reversal circuit.
- The bit reversal operation is performed by the shift registers in the FFT architecture by interleaving the data.
- Therefore, the proposed architecture requires a lower number of registers and has high throughput.

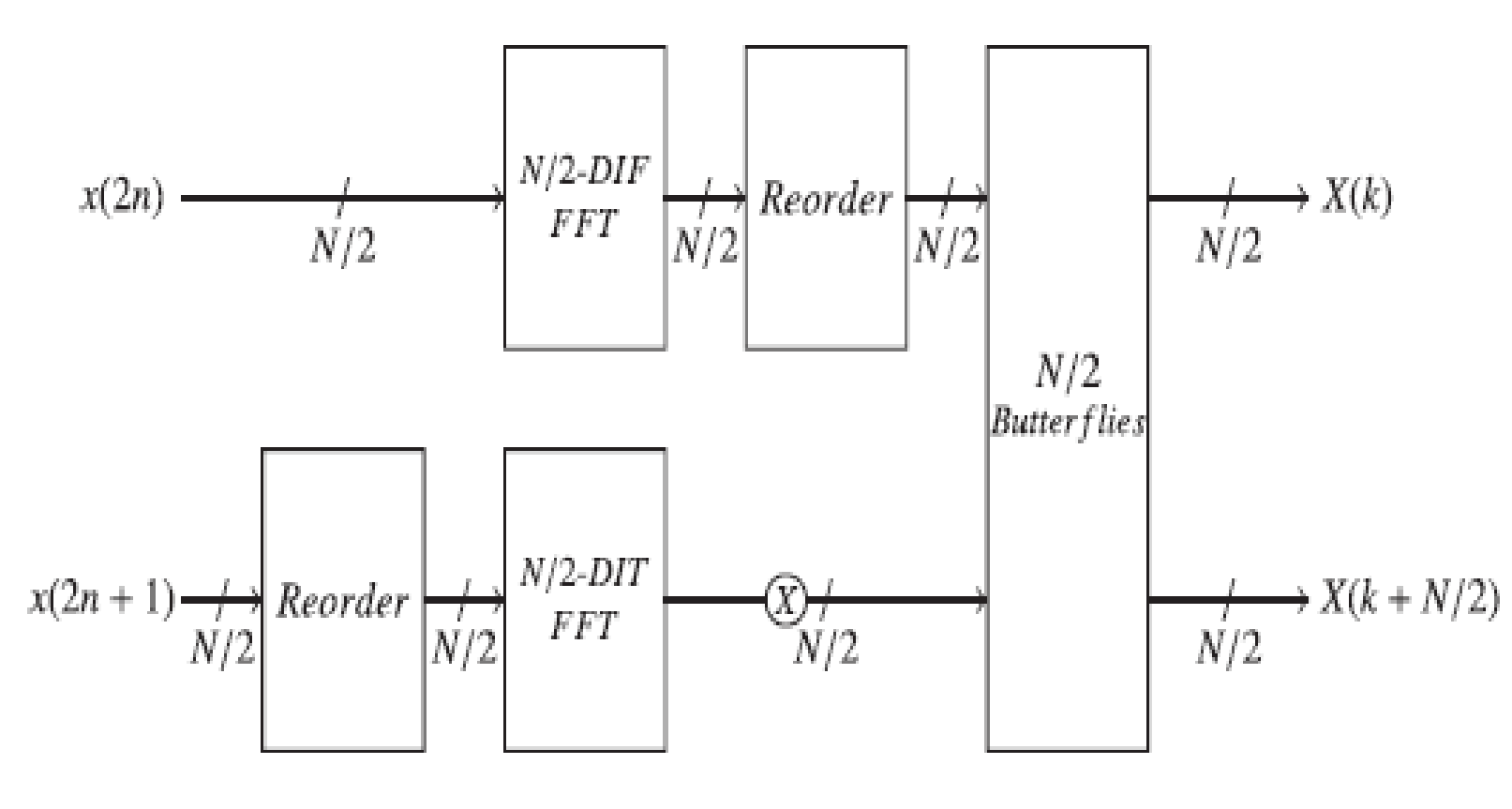
Existing block



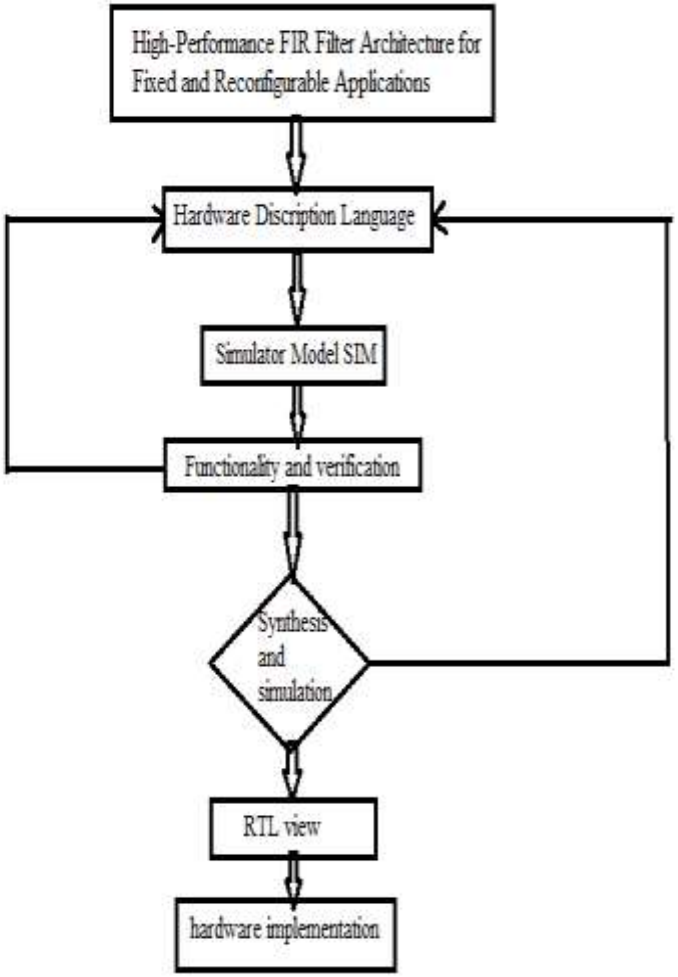
Proposed block

- The idea of computing an *N-point FFT using two N/2-point* FFT operations with additional one stage of butterfly operations is shown in the following slide which is not the exact architecture but provides the methodology.

Proposed block



Design flow


High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications
Hardware Discription Language
Simulator Model SIM
Functionality and verification
Synthesis and simulation
RTL view
hardware implementation

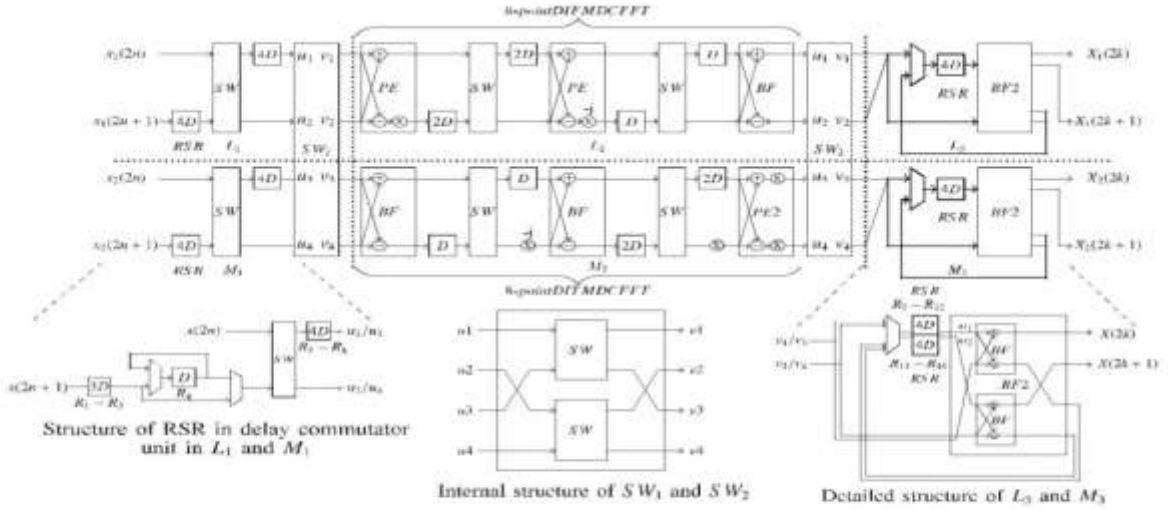


Fig. 2. Proposed 16-point radix-2 FFT architecture with outputs in natural order.

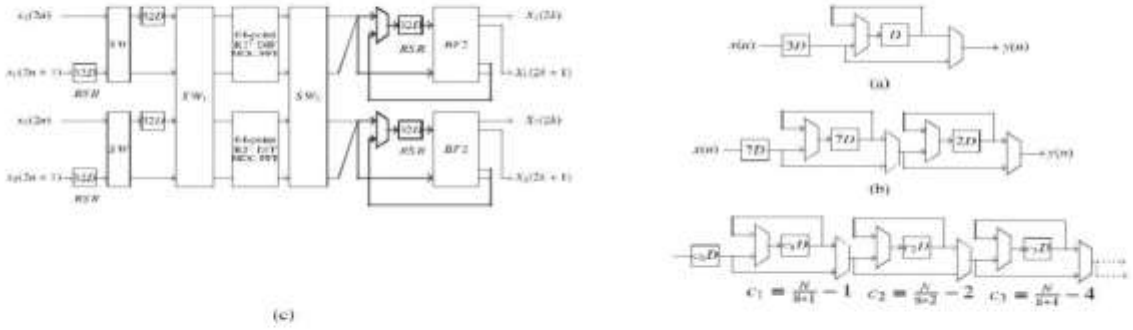
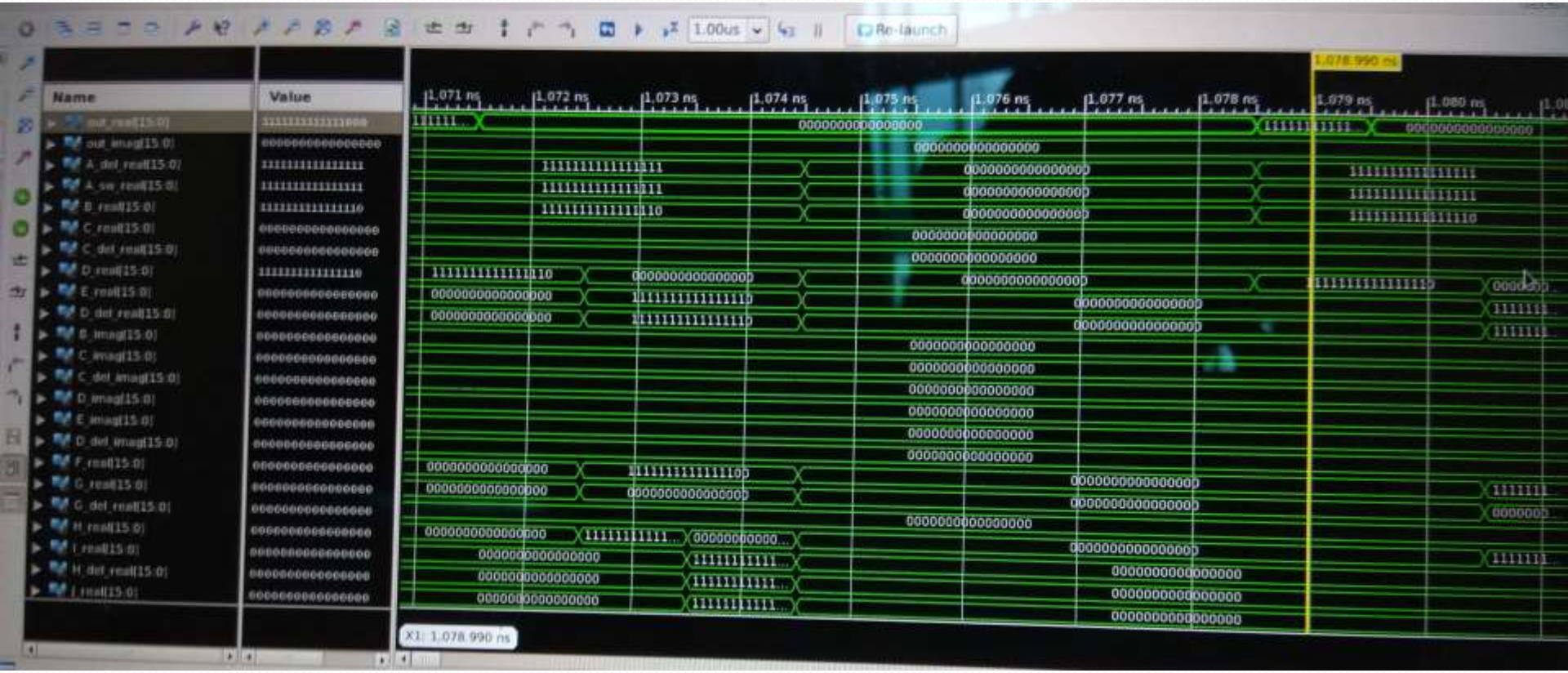


Fig. 3. Proposed 128-point radix-2^3 FFT architecture.

TABLE II

Output:


Re-launch
Name
Value
1.071 ns
1.072 ns
1.073 ns
1.074 ns
1.075 ns
1.076 ns
1.077 ns
1.078 ns
1.079 ns
1.080 ns
X1: 1.078.990 ns

Advantages

- Reduces area delay product.
- Reduces energy per sample.
- Reduces the cycle period.
- Reduces filter length.
- Reduces the complexity.
- High throughput reduces the number of additions

Applications

- digital signal processing applications,
- speech processing,
- loud speaker equalization,
- echo cancellation,
- adaptive noise cancellation

Extension

- Extension of A Normal IO Order Radix-2 to Radix-4

Tools used

- Software :- Xilinx
- Simulator:- ISE simulator 14.7

Refference

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